Morphing Machines

Reconfigurable Silicon Cores

REDEFINE ™

Reconfigurable Massively Parallel Processor SoC for High-Performance Embedded and Edge Computing

Reinventing cutting-edge silicon innovation in India ***morphing.in***

REDEFINE ™ Overview

REDEFINE ™ Technology

- **REDEFINE** – Scalable, customizable, power optimizing, reconfigurable massively parallel processor platform for building high-performance many-core SoC solutions for high-performance computing on the edge

REDEFINE System-on-Chip

- **REDEFINE** ***XNOC*** – Wide ***2-torus NoC interconnect*** provides high-performance ***priority-based*** deadlock-free routing, ***virtual channels***, and ***fault-tolerance***
- **Scalable and customizable** fabric of ***Compute Nodes*** – with each Compute Node providing an ensemble of Compute Cores, distributed memory, and Custom Function Units
- ***Global Resource Nodes*** add additional resources for bootstrapping, operating systems (including Linux and RTOSes), special CFUs, extended on-chip memory, run-time software control, and gateways to off-chip RAM and external peripheral interfaces
- Clock speeds of ***1 GHz and faster*** using ***28 nm and finer*** process nodes, regular structured layout enabling optimal validation and high silicon area utilization
- Scalable fabric from ***64 to 4,096 Compute Cores*** on a single SoC, 4 MB – 256 MB on-chip memory, from ***64 Gflop/s up to 4 Tflop/s*** peak compute capacity
- ***Compiler-assisted run-time power management*** for much higher power efficiency than GP-GPUs
- Support for ***standalone MPSoC mode*** with on-chip integrated RISC-V 32-bit or 64-bit main and control processors, or ***dedicated accelerator mode*** managed by external host processor over PCIe
- Hardware support for ***fast pre-emptive context switch and fabric re-partition***

REDEFINE Applications

- ***AI and Machine Learning*** – High-performance AI and ML applications in the cloud, at the core, or on the edge
- ***HPC on the Edge*** – Data analytics, stream processing, and other numerical applications in edge computing
- ***Embedded Real Time Systems*** – High-performance computing liberated from the data center and unleashed for use in embedded real-time systems for mixed-criticality applications

REDEFINE ™ *Compiler and Programming Model*

- Powerful LLVM based compiler framework ***enables rapid development of new applications*** using multiple parallel and sequential programming models including *OpenCL*
- ***Enables rapid re-targeting of existing application source code*** to the **REDEFINE** programming model API
- Uses a ***RISC-V 32-bit ISA*** (RV32IMF) based ***extended instruction set*** for the **REDEFINE** acceleration kernel binaries, with extended ***custom*** **REDEFINE** ***instructions for distributed computing orchestration*** on the compute fabric
- ***Simple and easy C programming API for direct data-flow driven parallel programming*** – supports explicit declarative programming of data-flow graphs elaborated either statically at launch of acceleration kernel instance or dynamically during kernel instance execution
- ***Automatic*** generation of ***hardware reconfiguration*** meta-data for the **REDEFINE** run-time system
- ***Supports parallel execution at multiple levels*** – Task Level Parallelism through concurrent execution of multiple acceleration kernels, Data Level Parallelism through dynamic data-flow driven scheduling and execution, and Instruction Level Parallelism through partitioning of the computation within a Compute Node

Artistic impression

Envisaged **REDEFINE** **64-Core** SoC
for Embedded and Edge HPC

Information on ***Morphing Machines*** IPs, products, solutions, and services is overleaf. More information is available at ***https://morphing.in***

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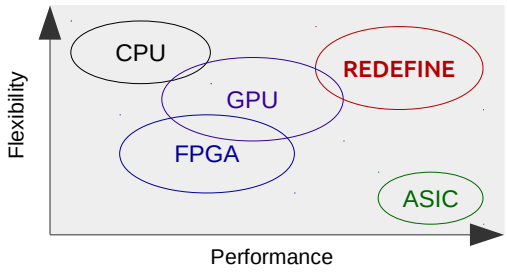
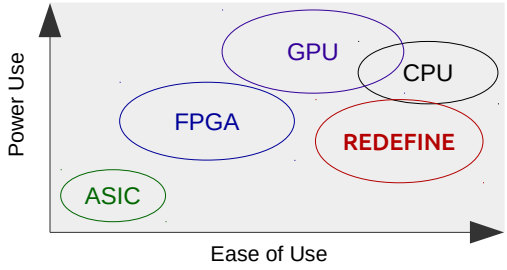
Why REDEFINE ™

- High performance like ASIC, high flexibility like GPP



- Low power like ASIC, high ease of use like GPP



- A single **REDEFINE** SoC accelerates multiple classes of compute-intensive algorithms

REDEFINE ™ Architecture

- High level architecture of a **64-Core REDEFINE** SoC

Real-time Systems Capability

- ***Software interrupt distribution*** to all running kernel instances ***within 8 µs*** (@ 1 GHz clock), and full-fabric software ***context-switch and re-partition in 4 ms*** (using DDR3 off-chip RAM)

About Morphing Machines

- ***Morphing Machines Pvt Ltd*** is a closely held fab-less semiconductor company launched from the ***Indian Institute of Science*** at Bangalore
- Led by highly distinguished alumni of IIT and IISc with decades of rich global experience in semiconductor, computer, communication, and software technology at world-leading computer and software corporations
- Emerging as one of India's most exciting new-generation cutting-edge IP-focused deep technology companies and featured in 2011 ***Gartner Cool Vendors (Semiconductor) Report***
- ***Top 50 finalist (Top 6 in Data & AI Track)*** of the Paris 2016 ***Hello Tomorrow*** Global Deep Technology Summit
- **REDEFINE** demonstrated and widely acclaimed at the 4th ***RISC-V Workshop at MIT*** in 2016

Upcoming REDEFINE ™ SoCs

- **RED-0464** – ***SoC for HPC on the edge*** – 4-core on-chip 32-bit or 64-bit Main Processors (Linux and/or RTOS capable), 32-bit Control Processors, **64 REDEFINE** compute cores (in clusters of 4 each at 16 compute nodes on a 4x4 2-torus NoC) (RV32IMFX*R*), 4 MB total on-chip distributed memory (256 KB per node) (L2 cache), 8 KB L1I and 8 KB L1D cache per compute core, 68 Gflop/s peak compute capacity @ 1GHz
- **RED-4256** – ***SoC for HPC at the core*** – 4-core on-chip 64-bit (RV64G ISA) Main Processors (Linux and RTOS capable), 32-bit Control Processors, **256 REDEFINE** compute cores (in clusters of 4 each at 64 nodes on a 8x8 2-torus NoC) (RV32IMFX*R*), 16 MB total on-chip distributed memory (256 KB per node) (L2 cache), 32 KB L1I and 32 KB L1D cache per compute core, 260 Gflop/s peak compute capacity @ 1 GHz
- Both the SoCs offer 1 GHz+ clock frequency, external interfaces (up to 16 GB off-chip DDR3 memory, USB3, PCIe4x16, gigE, 32–64 GPIO), @ 28 nm process node

Information on **REDEFINE** technology and silicon IP is overleaf. More information is available at ***https://morphing.in***

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