# REDEFINE Overview

## *REDEFINE* Technology

- ***REDEFINE*** – Scalable message-passing architecture and silicon platform for building runtime reconfigurable *polymorphic ASICs* and MPSoCs for *massively parallel processors and heterogeneous multi-core and many-core processors for compute-intensive applications*
- Compiler-supported dataflow-driven execution paradigm

## *REDEFINE* Silicon Platform

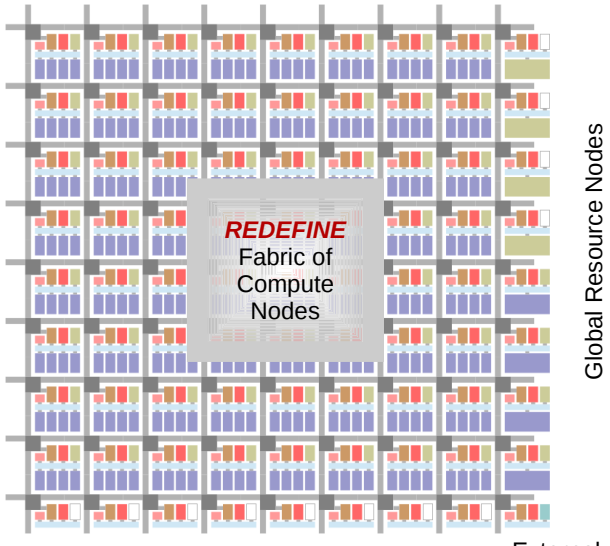
- ***REDEFINE XNOC*** – High-performance Network-on-Chip of packet routers providing deadlock-free routing and support for multiple topologies, virtual channels, fault-tolerance, and configurable data-paths and interfaces
- Scalable fabric of ***Compute Nodes*** – each Compute Node provides an ensemble of compute elements, distributed memory, and Standard or Custom Functional Units, with support for reuse of existing silicon IPs as Standard or Custom Functional Units
- ***Global Resource Nodes*** around the compute fabric provide additional resources for bootstrapping, special processing, extended memory, runtime orchestration, off-chip communication, and external host interfaces
- Clock speeds of 1 GHz and faster using 65nm and smaller process nodes in ASIC realizations, and up to 200 MHz on supported FPGAs
- Regular structured layout enabling optimal silicon area utilization in ASIC and FPGA realizations
- Scalable from 8 up to over 4,096 Compute Nodes
- Support for intelligent multi-level power management
- PCIe compliant external host interface (support for other interfaces in future)
- Support for standalone MPSoc realization with on-chip integrated RISC-V ISA based or other host processors

## *REDEFINE Simulators*

- Fast cycle-accurate ***REDEFINE Simulators*** generated by ***Chisel*** high-level Hardware Description Language
- Enables full functional verification of the hardware design (no more expensive RTL simulation needed), extensive pre-synthesis design validation, and complete application performance benchmarking – much before any hardware realization is available

## *REDEFINE Meta Compiler Framework*

- Enables developing new applications using multiple parallel and sequential programming models including standard parallel programming models such as *OpenCL*
- Enables re-targeting existing application sources (for supported programming languages) to a ***REDEFINE*** reconfigurable silicon core
- ***REDEFINE*** kernels use internal *program* representation adapted from the ***RISC-V*** *Instruction Set Architecture*
- Performs multi-level concurrency analysis, generates computational substructures (HyperOps) and hardware configuration meta-data for use by the ***REDEFINE*** runtime orchestration environment
- Supports parallel execution at multiple levels – Task Level Parallelism through concurrent execution of multiple acceleration kernels, Data Level Parallelism through pure dynamic dataflow driven scheduling and execution, and Instruction Level Parallelism through partitioning of the computation within a Compute Node
- Supports *stream* oriented programming models through dynamically reconfigurable custom data-paths




High level architecture of a ***REDEFINE*** massively parallel processor core with 256 compute elements

Information on ***Morphing Machines*** IPs, products, solutions, and services is overleaf. More information is available at ***http://morphing.in***



***Morphing Machines Pvt Ltd,*** *#17, 10A Main, 16 Cross, Malleshwaram, Bangalore 560 055, India*
*Email:* ***info@morphing.in*** *Phone/Fax: +91 80 4206 0618*

# Morphing Machines

***Reconfigurable Silicon Cores***

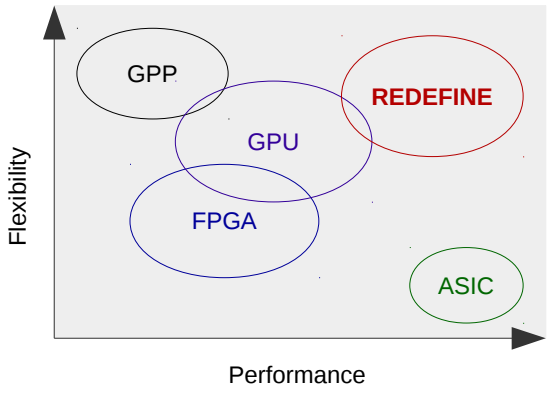
# REDEFINE ™

***Massively Parallel Processor Platform***

***Reinventing cutting-edge silicon innovation in India*** ***morphing.in***

## Why REDEFINE

- ***REDEFINE*** technology delivers high flexibility like a GPP with the high performance and low power of ASICs
- A single ***REDEFINE*** core accelerates an entire class of compute-intensive applications
- Much reduced NRE cost of complex MPSoC designs




Maximize flexibility and performance and minimize power with ***REDEFINE*** reconfigurable silicon cores

## REDEFINE Solutions

- ***REDEFINE ReCrypt*** – High-throughput silicon engine for runtime reconfigurable multi-protocol cryptography supporting AES and Elliptic Curve Cryptography
- ***REDEFINE XFloat*** – High-throughput silicon engine for floating-point linear algebra computations supporting double and extended precision arithmetic, special functions, and vector and matrix operations kernels
- ***REDEFINE XFace*** – High-performance silicon engine for face recognition applications
- ***REDEFINE XANN*** – High-performance heterogeneous multi-core engine for Radial Basis Function based multi-layer neural network classifier applications
- ***REDEFINE AVAC*** – High-performance reliable silicon engine for reconfigurable on-board computing systems for aviation applications
- Many other ***REDEFINE*** accelerator solutions are currently under research and development by ***Morphing Machines*** and its partners in the areas of simulation, computer vision, software defined radio, software defined networking, neural networks, and bioinformatics

## About Morphing Machines

- ***Morphing Machines Pvt Ltd*** is a closely held fabless semiconductor company launched from the Technology Entrepreneurship Initiative of the ***Indian Institute of Science*** at Bangalore, India
- Emerging as one of India's most exciting cutting- edge IP focused technology start-up companies, ***Morphing Machines*** featured as one of the four global start-up semiconductor companies in the ***Cool Vendors 2011*** report of ***Gartner Research***
- Founded by a group of distinguished IIT and IISc alumni with decades of rich experience at world- leading semiconductor, computer, communication, and software technology corporations
- Working in close collaboration with research groups at th***e Indian Institute of Scien***ce at Bangalore, ***Morphing Machines*** has created an exciting portfolio of ***reconfigurable silicon cores***

## Other Key MM Offerings

- ***MM REMoSS*** – (Reconfigurable Embedded Monitor for Secure Systems) – Secure application execution environment for FPGA based embedded system and MPSoC applications systems and solutions
- ***MM CONVERSE*** – (Concurrent Verilog Simulation Environment) – Massively parallel, scalable, high-performance Verilog RTL simulation environment for ***REDEFINE*** processors and GPUs
- ***MM RFFT and LPFFT*** – Reconfigurable and low-power high-performance silicon IPs for up to 64K point FFT
- ***MM RAES*** – Reconfigurable high-performance silicon IPs for AES encryption/decryption supporting up to 256-bit AES key lenghts in standard and custom AES modes
- ***MM RECC*** – Reconfigurable high-performance silicon IP for generalized finite field arithmetic with ready-to-use Elliptic Curve Cryptography support
- ***MM SHARC*** – Optimized silicon IPs for very fast secure hash function units

Information on ***REDEFINE*** technology and silicon IP is overleaf. More information is available at ***http://morphing.in***



***Morphing Machines Pvt Ltd,*** *#17, 10A Main, 16 Cross, Malleshwaram, Bangalore 560 055, India*
*Email:* ***info@morphing.in*** *Phone/Fax: +91 80 4206 0618*